REMARKS

Applicant concurrently files herewith a Three-Month Extension of Time and a Notice of Appeal.

Claims 3-9, 11-18, 20-22, and 24-25 are all the claims presently pending in the application. Claims 19 and 23 have been canceled without prejudice or disclaimer.

Claims 11, 12, 16 and 17 stand rejected under 35 U.S.C. § 112, first and second paragraphs. The specification has been amended to clarify that dummy gate electrodes may be arranged on element isolation regions. Applicant notes that such features were included in the claims as filed originally and therefore are part of the original disclosure. Therefore, no new matter has been added. Further, claim 12 has been amended above to provide antecedent basis to a first transistor and a second transistor.

Entry of this §1.116 Amendment is proper. Since the amendments above narrow the issues for appeal and since such features and their distinctions over the prior art of record were discussed earlier, such amendments do not raise a new issue requiring a further search and/or consideration by the Examiner. As such, entry of this Amendment is believed proper and is earnestly solicited. No new matter has been added.

It is noted that the claims have been amended solely to more particularly point out Applicant's invention for the Examiner, and not for distinguishing over the prior art, narrowing the claim in view of the prior art, or for statutory requirements directed to patentability.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached pages are captioned "**Version with markings to show changes made**".

Claims 3, 5, 14, 15, 18, 20-22, and 24-25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bush, et al. (U.S. Patent No. 5,986,283) (hereinafter "Bush").

Claims 4 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over

Bush et al., and further in view of Ham (U.S. Patent No. 5,977,595) (hereinafter "Ham"). .

Claims 6-8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mizuno, et al. (U.S. Patent No. 6,140,686) (hereinafter "Mizuno"), and in view of Lin, et al. (U.S. Patent No. 5,932,900) (hereinafter "Lin").

Claims 9, 11, 12, 16, and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mizuno, et al., in view of Lin, et al., and further in view of Uehara, et al. (U.S. Patent No. 5,946,563) (hereinafter "Uehara").

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed (for example, by independent claim 3 and substantially similarly by independent claims 5, 6, and 11), is directed to a semiconductor device.

The invention was described in the Amendment filed on November 26, 2001, and for convenience the Examiner is referred thereto.

As discussed in the Amendment of November 26, 2001, the exemplary semiconductor device includes a first transistor having a first gate put between a first source and a first drain, a second transistor arranged adjacent to the first transistor, the second transistor having a second gate put between a second source and a second drain, a first dummy gate arranged between the first drain and the second source, a second dummy gate arranged adjacent to the first source, and a third dummy gate arranged adjacent to the second drain. The first and second gates, and the first, second and third dummy gates are evenly spaced. In the structure of the invention the first dummy gate is arranged parallel to the first gate. Further, a first electrode layer is a source of a first transistor and the second electrode layer is a drain of the first transistor.

An exemplary configuration of the optical amplifying medium of the invention is shown in Figs. 1-3 of the application.

The conventional systems, such as those discussed below and in the Related Art section of the present application, do not have such a structure, and fail to provide for such an

operation.

Indeed, such features are clearly not taught or suggested by the cited references.

II. THE PRIOR ART REJECTIONS

A. The U.S.C. § 103(a) Rejection Based on Bush

The Examiner asserts:

> *[regarding claims 3, 5, 14, 15, and 18-25] Bush discloses (see, for example, FIG. 5) a test structure comprising gate conductors (first and second gate) 20 and conductors (first and second dummy gate) 40. The first transistor (the second from the left in FIG. 5 of Bush) possesses a first gate 20, first source region 22 and first drain region 24 and is spaced from a first dummy gate (the third from the left) 40. The first dummy gate is laterally spaced from a second transistor (on the far right) possessing a second gate 20 , second source region 22 and second drain region 24. The second dummy gate 40 (on the far left) lies outside the first source regions and the first drain region. The first and second gates, and said first, second dummy gates are evenly spaced. Bush does not show a third dummy gate arranged adjacent to said second drain. However, it would have been obvious to one of ordinary skill in the art at the time of invention to include an additional dummy gate with more transistors in order to test more transistors within a single test structure.*

However, Applicant respectfully disagrees.

Firstly, the assertions by the Examiner on page 3, item 7 of the Office Action are very general. The Examiner does not indicate specifically which of the conductors 40 correspond to a first and second dummy gate of the invention nor which conductors 20 correspond to a first and second gate of the invention.

In the present invention, a structure in a non-limiting embodiment includes a first transistor having a first gate between a first source and a first drain. Further, a second transistor is arranged adjacent to the first transistor and includes a second gate between a

second source and a second drain. The second gate is arranged parallel to the first gate. Also, a first dummy gate is arranged between the first drain and the second source and is parallel to the first gate. Thus, as shown for example in Fig. 1 of the invention, the first dummy gate is parallel to a first gate of a first transistor and, therefore may also be parallel to the second gate of the second transistor.

In contrast, even assuming that conductors 40 corresponds to a first and second dummy gate as asserted by the Examiner, the conductors 40 are not parallel to gate conductors 20. Instead, a distal end of gate conductors 20 is opposed to a distal end of conductors 40.

As shown in Fig. 5 of Bush, there is no teaching or suggestion of the novel features of the claimed invention. Specifically, Bush does not teach or suggest that a first conductor 40 (e.g., asserted to be a dummy gate) is parallel to a first conductor 20 and to a second conductor 20. Further, Bush does not teach or suggest that a dummy gate is disposed between the first and second transistors nor between the first drain and a second source. That is while conductors 40 are between multiple sources 22 they are not between drains 24. Instead, conductors 40 are across from drains 24.

Hence, turning to the clear language of the claims, there is no teaching or suggestion of "*[a] semiconductor device, comprising:*

a first transistor having a first gate put between a first source and a first drain;

a second transistor arranged adjacent to said first transistor, said second transistor having a second gate put between a second source and a second drain;

a first dummy gate arranged between said first drain and said second source;

a second dummy gate arranged adjacent to said first source; and

a third dummy gate arranged adjacent to said second drain,

wherein said first and second gates, and said first, second and third dummy gates are substantially evenly spaced, and

wherein said first dummy gate is arranged parallel to said first gate" (emphasis Applicant's), as exemplarily defined by independent claim 3 (and similarly independent claim 5). Thus, all of claims 1, 5, 14, 15, 18, 20-22 and 24-25 are patentable.

B. The § 103 Rejection Based on Mizuno in view of Lin

The Examiner alleges that Mizuno would have been combined with Lin to form the claimed invention. However, Applicant respectfully submits that these references would not have been combined and even if combined (arguendo), the combination would not teach or suggest the claimed invention.

Independent claim 6 as amended above recites "*...wherein said first electrode layer is a source of said first transistor and said second electrode layer is a drain of said first transistor*" (emphasis Applicant's).

On the other hand, Mizuno fails to teach or suggest such a relationship and only discloses in Fig. 21 a single layer which is either a "source/drain of NMOS" or "source/drain of PMOS" and not the claimed relationship. Further, Lin fails to make up for the deficiencies of Mizuno and thus even if combined (arguendo), Mizuno and Lin fail to teach or suggest "*said first electrode layer is a source of said first transistor and said second electrode layer is a drain of said first transistor*".

Thus, for the reasons stated above claim 6 (and dependent claims 7-8) of the claimed invention are fully patentable over the cited references.

Further, the other prior art of record has been reviewed, but it too even in combination with Mizuno and Lin fails to teach or suggest the claimed invention.

C. The § 103 Rejection Based on Mizuno in view of Lin and Uehara

The Examiner alleges that Uehara would have been combined with Mizuno and Lin to form the claimed invention. However, Applicant respectfully submits that these references also would not have been combined and even if they were combined (arguendo), the combination would not teach or suggest the claimed invention.

Independent claim 11 recites "*...a first gate electrode formed between said first source and drain diffusion regions and extending in a second direction;*

a second gate electrode formed between said second source and drain diffusion regions and extending in said second direction" (emphasis Applicant's). Further, such a

second direction is clearly shown in Fig. 2 of the present invention in which first pair transistors 4A and second pair transistors 4B extend in a second direction different from that of the first line which includes the first source diffusion region, the first drain diffusion region, the second source diffusion region, and the second drain diffusion region.

As shown in Fig. 21 of Mizuno there is no teaching or suggestion of a first and second direction as defined by independent claim 11 of the present invention. Further, Lin and Uehara, even if combined (arguendo) with Mizuno do not make-up for the deficiencies of Mizuno with regards to the first and second directions. Thus, for the reasons stated above, independent claim 11 (and dependent claims 9, 12, 16, and 17) are fully patentable over the cited references.

D. The § 103 Rejection Based on Bush and in view of Ham

The Examiner alleges that Bush would have been combined with Ham to form the claimed invention. However, Applicant respectfully submits that these references, similar to those above, would not have been combined and even if they were combined (arguendo), the combination would not teach or suggest the claimed invention.

Specifically, Applicant submits that claims 4 and 13 also provide additional limitations, which in combination with those of independent claim 3, are neither taught nor suggested by Bush and Ham.

For example, neither Bush nor Ham teach or suggest, even if they were to be combined (arguendo), a semiconductor device "*wherein said first dummy gate is arranged parallel to said first gate*". Therefore, Bush either alone or in combination with Ham is much different from the present invention and fails to teach or suggest the unique and novel features of the claimed invention.

Further, the other prior art of record has been reviewed, but it too, even in combination with Bush, Ham, Mizuno, Lin, and Uehara, fails to teach or suggest the claimed invention.

III. FORMAL MATTERS AND CONCLUSION

In response to the Examiner's objection to the Drawings, Applicant files herewith a Submission of Proposed Drawing Corrections for Figs. 1-3 marked in red to show an element isolation region 50. Further, Figs. 6-8 have been marked in red and labeled as "Prior Art". Further, in response to the Examiner's objection to the Drawings (e.g., on page 2, item 3 of the Office Action), Applicant respectfully notes that the specification has been corrected in the Amendment filed on November 26, 2001 to clearly identify the source diffusion region 7.

In view of the foregoing, Applicant submits that claims 3-9, 11-18, 20-22, and 24-25, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 8/14/02

8/14/02

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Fig.1

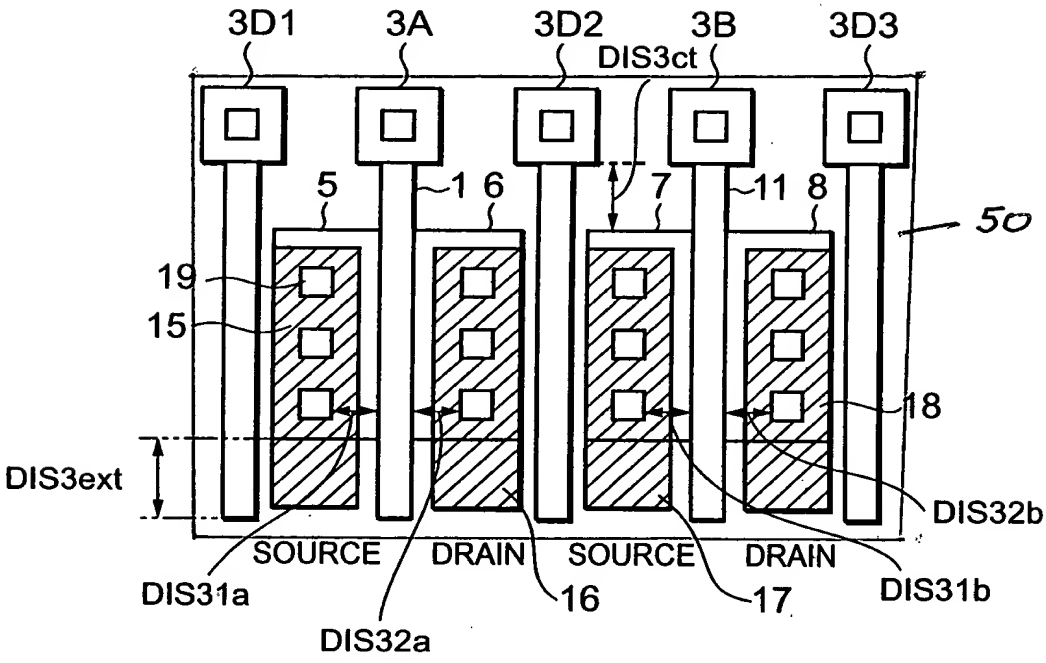


Fig.2

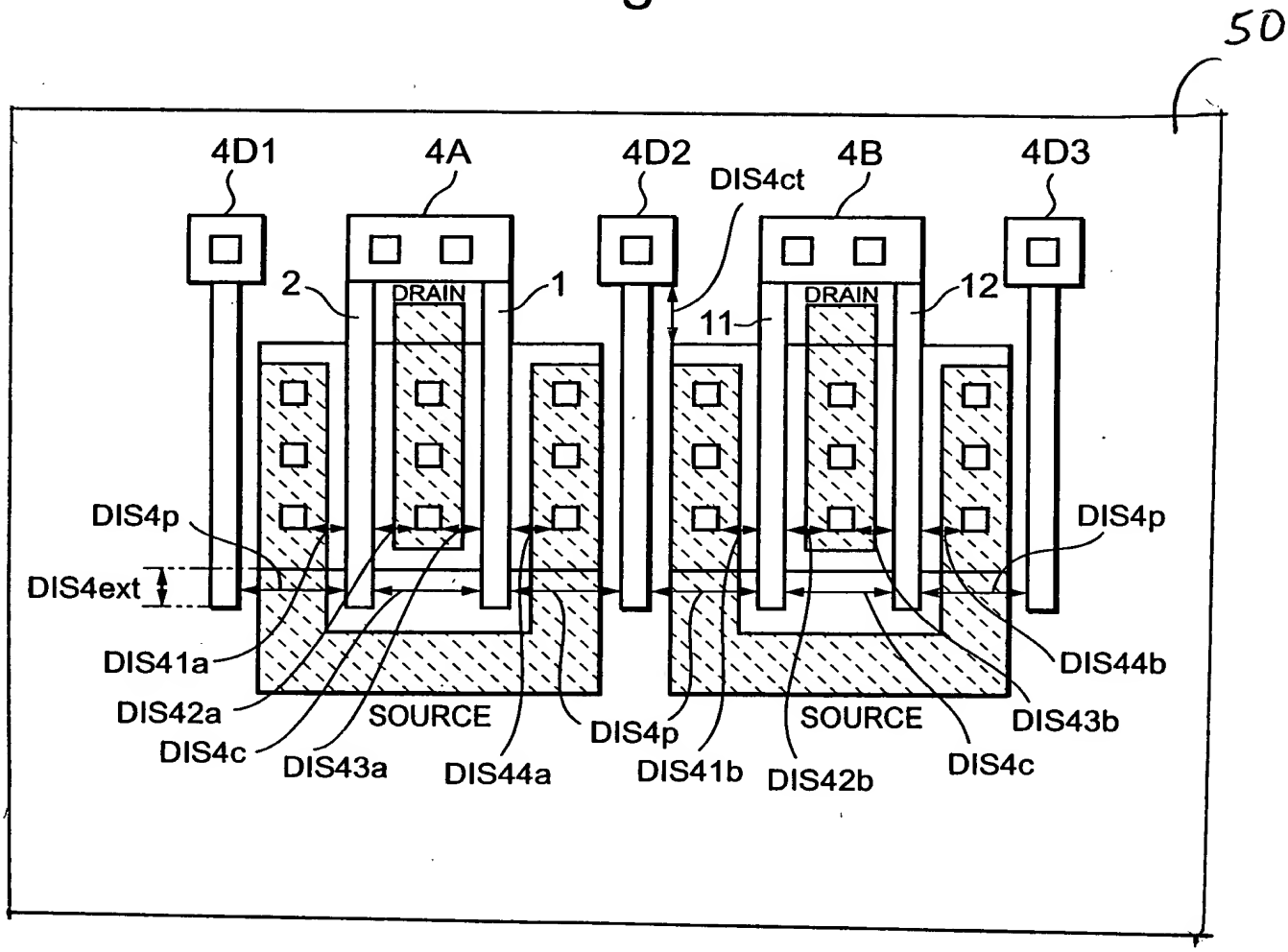
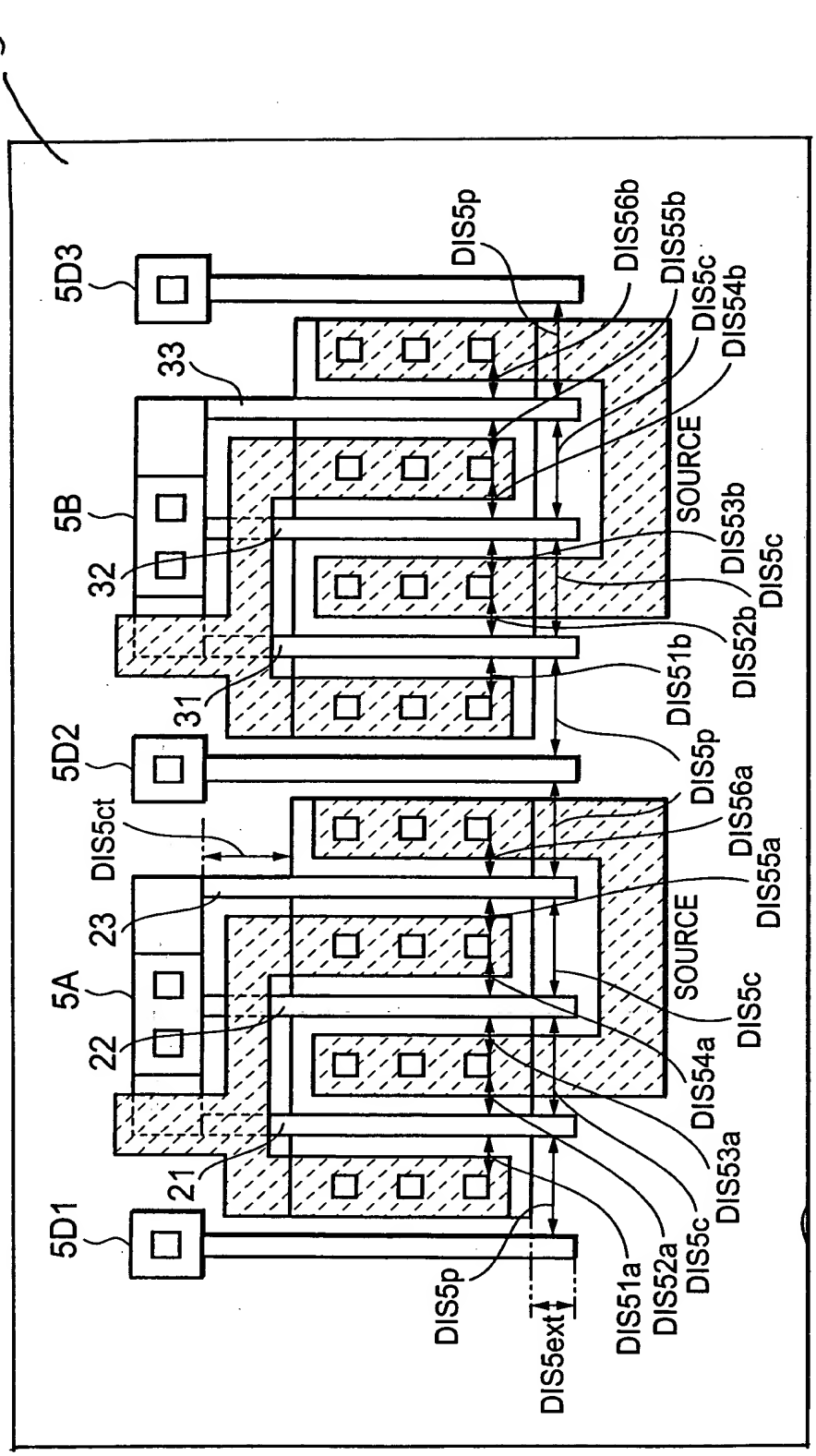


Fig.3



PRIOR ART

Fig.6

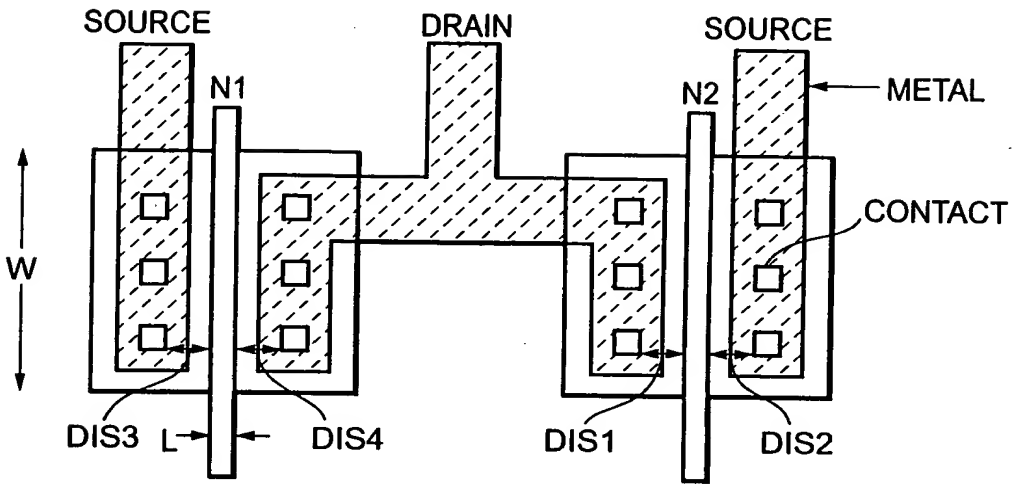


Fig.7

PRIOR ART

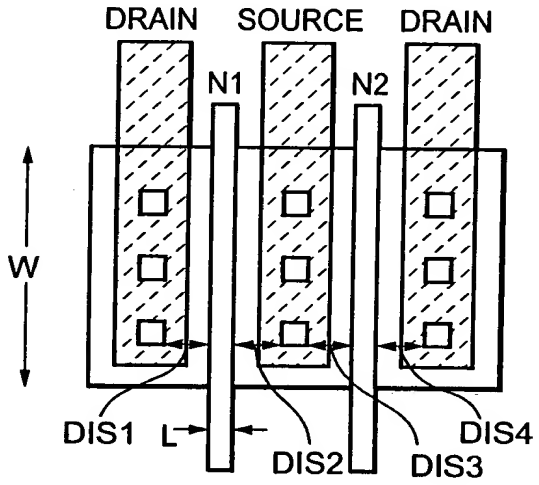


Fig.8

PRIOR ART